Notice of Allowability	Application No. 09/779,353	Applicant(s) PINO ET AL.	
	Examiner Herng-der Day	Art Unit 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendments received 4/6/05 and 5/11/05*.

2. ☒ The allowed claim(s) is/are *1, 2-18, now renumbered as 1-17*.

3. ☒ The drawings filed on *06 April 2005 and 11 May 2005* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *05112005* .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Thai Phan
Primary Examiner
AU: 2128

DETAILED ACTION

1. This communication is in response to Applicants' Amendment to Office Action dated January 6, 2005, faxed April 6, 2005, and Applicants' Supplemental Amendment faxed May 11, 2005.

1-1. Claims 1, 8, 9, and 18 have been amended. Claim 2 has been cancelled. Claims 1 and 3-18 are pending.

1-2. Claims 1 and 3-18 have been examined and allowed.

Reasons for Allowance

2. The following is an Examiner's statement of reasons for allowance:

2-1. The closest prior art of record discloses:

(1) A microprocessor having a DSP and a CPU and a decoder discriminating between DSP-type instructions and CPU-type instructions (Ohsuga et al., U.S. Patent 6,434,690 B1).

(2) An emulation system for emulating CPU core (Yamaura et al., U.S. Patent 5,594,890).

(3) A method for emulating a peripheral device (Bonola, U.S. Patent 5,953,516).

2-2. Independent claim 1 is directed at an emulating interface arrangement as shown in FIG. 1. This independent claim identifies the distinct combination of features of "a Programmable Logic Device (PLD) mounted on said bridge board and electrically connected to both said processor connection and said DSP connection", software included in said PLD converting signals into DSP transfer signals or processor transfer signals, and "said bridge board with said

PLD and said software emulate a physical and electrical connection between a processor and a DSP in an Application Specific Integrated Circuit (ASIC)".

Because the closest prior art does not teach or suggest an emulating interface arrangement for a processor evaluation board and a DSP evaluation board having connectors corresponding to actual data lines, address lines, and control lines of the emulated processor and DSP respectively to emulate an ASIC, claim 1 is deemed allowable.

Dependent claims 3-7 are allowable as they depend on the allowed independent claim 1.

2-3. Independent claim 8 is directed at an emulating interface arrangement as shown in FIG. 1. This independent claim identifies the distinct combination of features of "a Programmable Logic Device (PLD) mounted on said bridge board and electrically connected to both said processor connection and said DSP connection", software included in said PLD converting signals into DSP transfer signals or processor transfer signals, and "said control lines include an interrupt line, a wait line, and a clock line".

Because the closest prior art does not teach or suggest an emulating interface arrangement for a processor evaluation board and a DSP evaluation board having connectors corresponding to actual data lines, address lines, and control lines of the emulated processor and DSP respectively and said control lines include an interrupt line, a wait line, and a clock line, claim 8 is deemed allowable.

2-4. Independent claim 9 is directed at an emulating interface arrangement as shown in FIG. 1. This independent claim identifies the distinct combination of features of "a Programmable Logic Device (PLD) mounted on said bridge board and electrically connected to both said processor connection and said DSP connection", software included in said PLD converting

signals into DSP transfer signals or processor transfer signals, "said processor evaluation board emulating the operation of a processor", and "said DSP evaluation board emulating the operation of a DSP".

Because the closest prior art does not teach or suggest an emulating interface arrangement for a processor evaluation board and a DSP evaluation board having connectors corresponding to actual data lines, address lines, and control lines of the emulated processor and DSP respectively to emulate the operation of a processor and a DSP, claim 9 is deemed allowable.

Dependent claims 10-17 are allowable as they depend on the allowed independent claim 9.

2-5. Independent claim 18 is directed at an ASIC software emulator arrangement as shown in FIG. 1. This independent claim identifies the distinct combination of features of "a TMS320 evaluation board with signal lines corresponding to actual signal lines of TMS320 processor", "a TMS470 evaluation board with signal lines corresponding to actual signal lines of TMS470 processor", and "a bridge board connected to said signal lines of said TMS470 evaluation board and said TMS320 evaluation board" converting data between said processor format and DSP format.

Because the closest prior art does not teach or suggest an emulator arrangement with a TMS320 evaluation board and a TMS470 evaluation board for an ASIC emulator, claim 18 is deemed allowable.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30. Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: (571) 272-2100.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Jean R. Homere can be reached on (571) 272-3780. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Herng-der Day H.D.
May 11, 2005

Vhayphan
Patent Examiner
AU: 2128